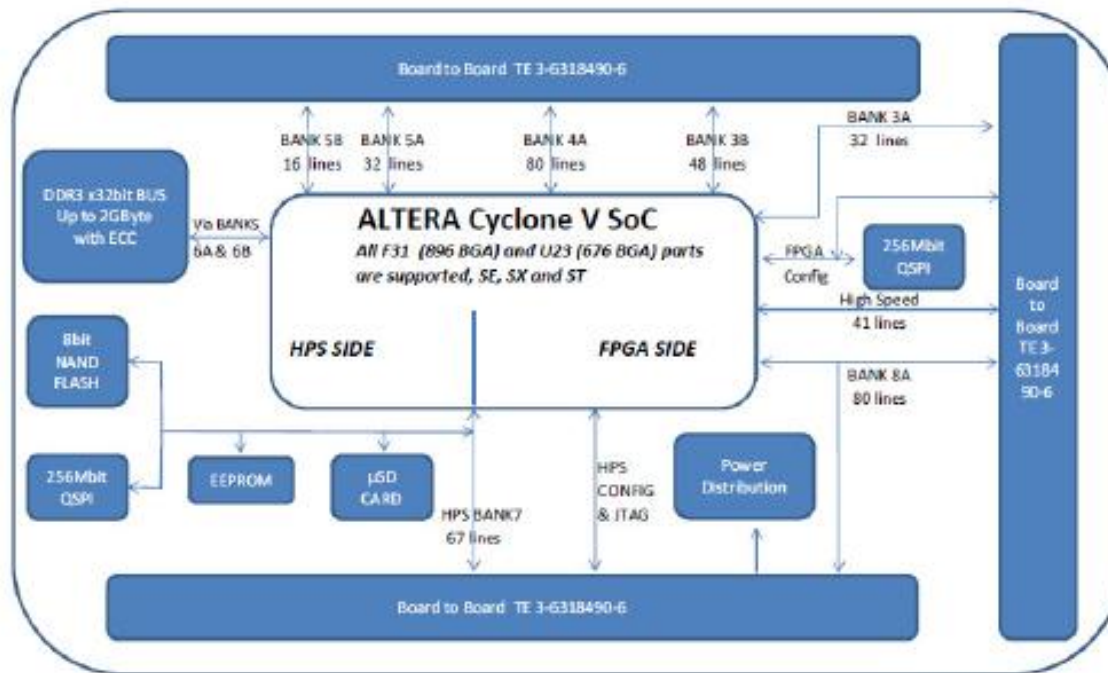


LLRF Hardware Platform based on System on Module(SOM) FPGA

P. Varghese

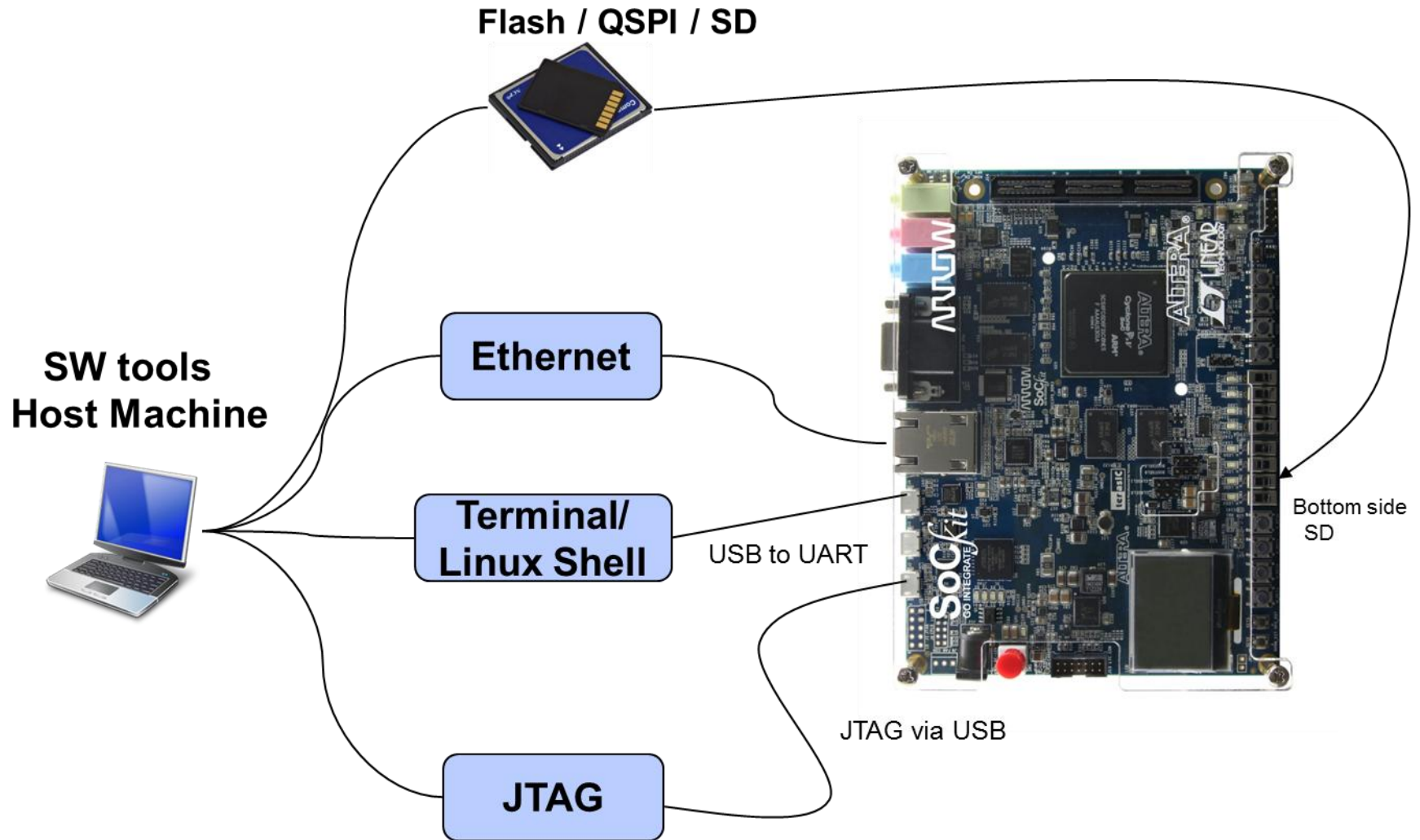
System on a Module (SOM)





- 2Gbyte DDR3
- 64Mbyte QSPI FLASH for HPS boot
- µSD slot connected to HPS
- 64Mbyte QSPI FLASH for FPGA boot
- Three Board to Board connectors, 220 Pins each
- Carrier Board has mating connector, TYCO TE 318272536

Debug Interfaces



DS-5 Debugger for ARM

The screenshot displays the DS-5 Debugger for ARM interface within the Eclipse Platform. The main window is titled "DS-5 Debug - HPS/linux-bringup/drivers/gpio/gpio-altera.c - Eclipse Platform".

Left Panel: Shows the "Debug Cont" tab with "Altera SoC FPGA connected" and "Active Threads". The threads list includes "blinkly #4 stopped on breakpoint #2 (PID 481 w)", "arch_local_irq_save", "altera_gpio_set+0x8", "gpio_set_value_cansleep+0x6C", "gpio_value_store+0xC0", "dev_attr_store+0x18", "flush_write_buffer+0x40", "sysfs_write_file+0x108", "vfs_write+0xA4", "sys_write+0x40", and "C:\N8000E700".

Top Center Panel: Shows the "Commands" tab with a list of commands: "wait", "continue", "Execution stopped at breakpoint 2: S:0x7F000038", "In thread 2 (OS thread id 479)", "S:0x7F000038 85,0 {", "wait", "continue", "Execution stopped at breakpoint 2: S:0x7F000038", "In thread 3 (OS thread id 478)", "S:0x7F000038 85,0 {", "wait", "continue", "Execution stopped at breakpoint 2: S:0x7F000038", "In thread 4 (OS thread id 481)", "S:0x7F000038 85,0 {".

Top Right Panel: Shows the "Breakpoints" tab with a list of breakpoints: "altera_gpio_get", "altera_gpio_set", "altera_gpio_dir_in", "altera_gpio_dir_out", and "altera_gpio_save_regs".

Bottom Left Panel: Shows the "gpio-altera.c" source code with the following content:

```
78 * @gpio: GPIO signal number.
79 * @val: Value to be written to specified signal.
80
81 * This function writes the specified value in to the
82 * GPIO device.
83 */
84 static void altera_gpio_set(struct gpio_chip *gc, unsigned long val)
85 {
86     unsigned long flags;
87     struct of_mm_gpio_chip *mm_gc = to_of_mm_gpio_chip(gc);
88     struct altera_gpio_instance *chip = to_altera_gpio_instance(gc);
89
90     spin_lock_irqsave(&chip->gpio_lock, flags);
91
92     /* Write to shadow register and output */
93     if (val)
94         chip->gpio_state |= 1 << gpio;
95     else
96         chip->gpio_state &= ~(1 << gpio);
97     __raw_writel(chip->gpio_state, mm_gc->regs + ALTERA_GPIO_REG);
98
99     spin_unlock_irqrestore(&chip->gpio_lock, flags);
100 }
101
102 /*
```

Bottom Center Panel: Shows the "Disassembly" tab with a list of instructions:

Address	Opcode	Disassembly
S:0x7F000024	15903050	LDRNE r3,[r0,#0x50]
S:0x7F000028	E5933000	LDR r3,[r3,#0]
S:0x7F00002C	E1A01133	LSR r1,r3,r1
S:0x7F000030	E2010001	AND r0,r1,#1
S:0x7F000034	E12FFF1E	BX lr
S:0x7F000038	E10F3000	altera_gpio_set
S:0x7F00003C	F10C0080	CPSID i
S:0x7F000040	E3A0C001	MOV r12,#1
S:0x7F000044	E3520000	CMP r2,#0
S:0x7F000048	E5902054	LDR r2,[r0,#0x54]
S:0x7F00004C	1182111C	ORRNE r1,r2,r12,LSL r
S:0x7F000050	01C2111C	BICEQ r1,r2,r12,LSL r
S:0x7F000054	E5902050	LDR r2,[r0,#0x50]
S:0x7F000058	E5801054	STR r1,[r0,#0x54]
S:0x7F00005C	E5821000	STR r1,[r2,#0]
S:0x7F000060	E121F003	MSR CPSR_c,r3
S:0x7F000064	E12FFF1E	BX lr
S:0x7F000068	E52D4004	altera_gpio_dir_in
S:0x7F00006C	E52D4004	PUSH {r4}

Bottom Right Panel: Shows the "Variables" tab with a list of variables:

Name	Value	Type	Count	Size	Location
Locals	1 variable				
flags	27	long unsigned int	32	SR3	
File Statics (current)					
Globals	954 variables				

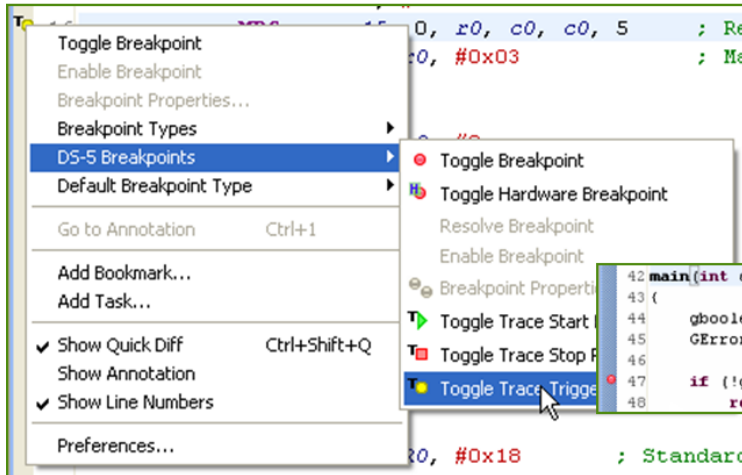
Bottom Right Panel (continued): Shows the "Variables" tab with a list of variables:

Name	Value	Size	Access
sptimer0			
sptimer1			
stm			
sysmgr			
uart0			
uart1			
usb0			
usb1			
PIO_inst_0			
PIO_inst_0_DATA	0x00000000	32	R/W
PIO_inst_0_DIRECTION	0x00000000	32	R/W
PIO_inst_0_IRQ_MASK	0x00000000	32	R/W
PIO_inst_0_EDGE_CAP	0x00000000	32	R/W
PIO_inst_0_SET_BIT	write only	32	WO
PIO_inst_0_CLEAR_BITS	write only	32	WO
UART_inst_0			
JTAG_UART_inst_0			
SYSID_inst_0			

Bottom Panel: Shows the "Writable" tab with a list of variables: "Writable", "Smart Insert", and "86:25".

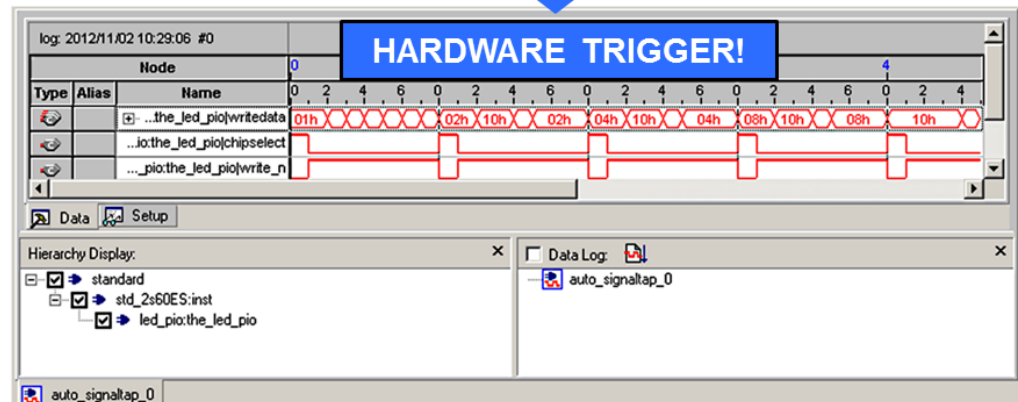
Cross Domain Debug1

■ Trigger from software to FPGA

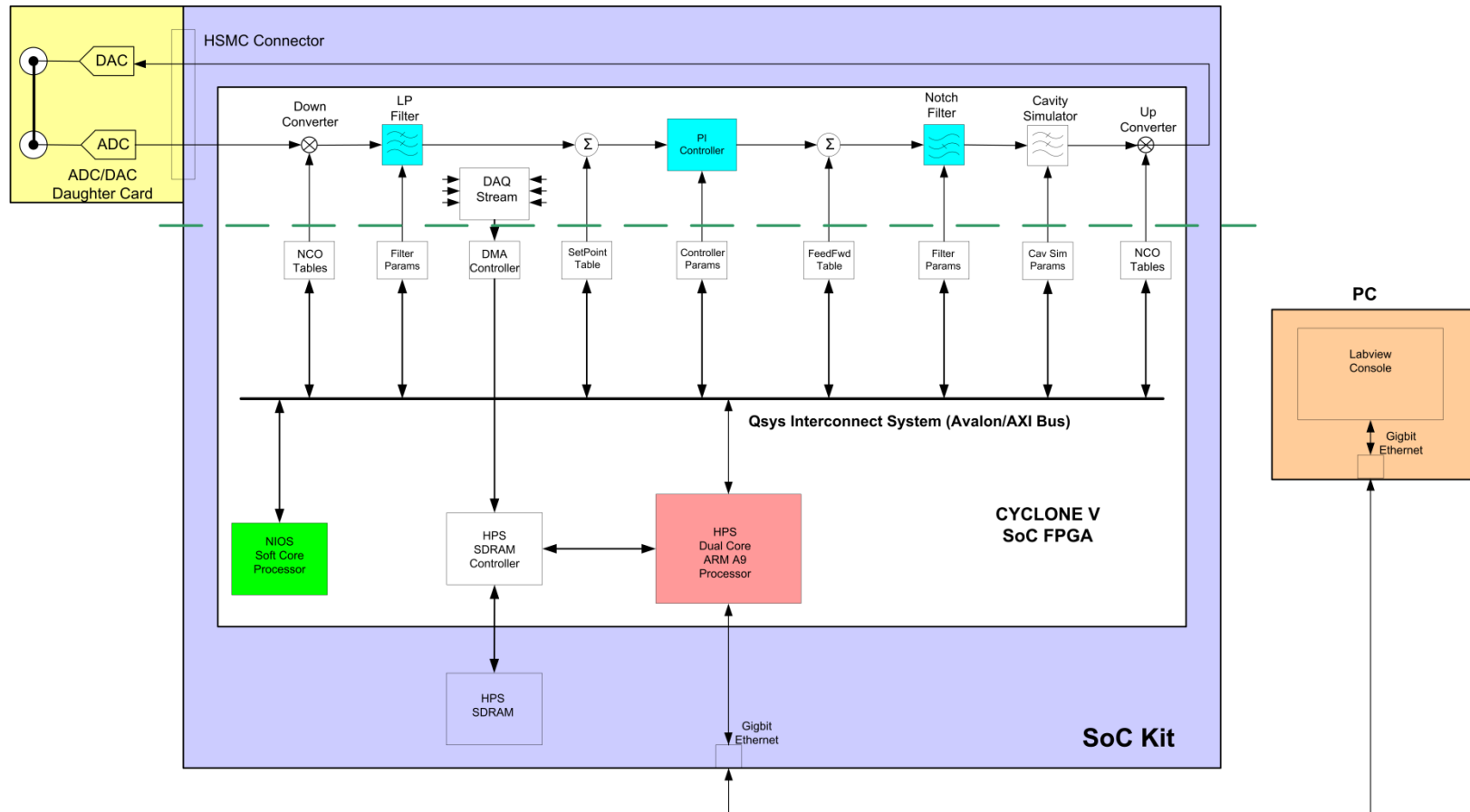


The screenshot shows a debugger's breakpoint menu. The 'DS-5 Breakpoints' sub-menu is open, and 'Toggle Trace Trigger' is highlighted. Other options include 'Toggle Breakpoint', 'Toggle Hardware Breakpoint', 'Resolve Breakpoint', 'Enable Breakpoint', 'Breakpoint Properties...', 'Toggle Trace Start', 'Toggle Trace Stop', and 'Toggle Trace Trigger'. A blue box with the text 'SOFTWARE TRIGGER OR BREAKPOINT TRIGGER' is positioned to the right of the menu.

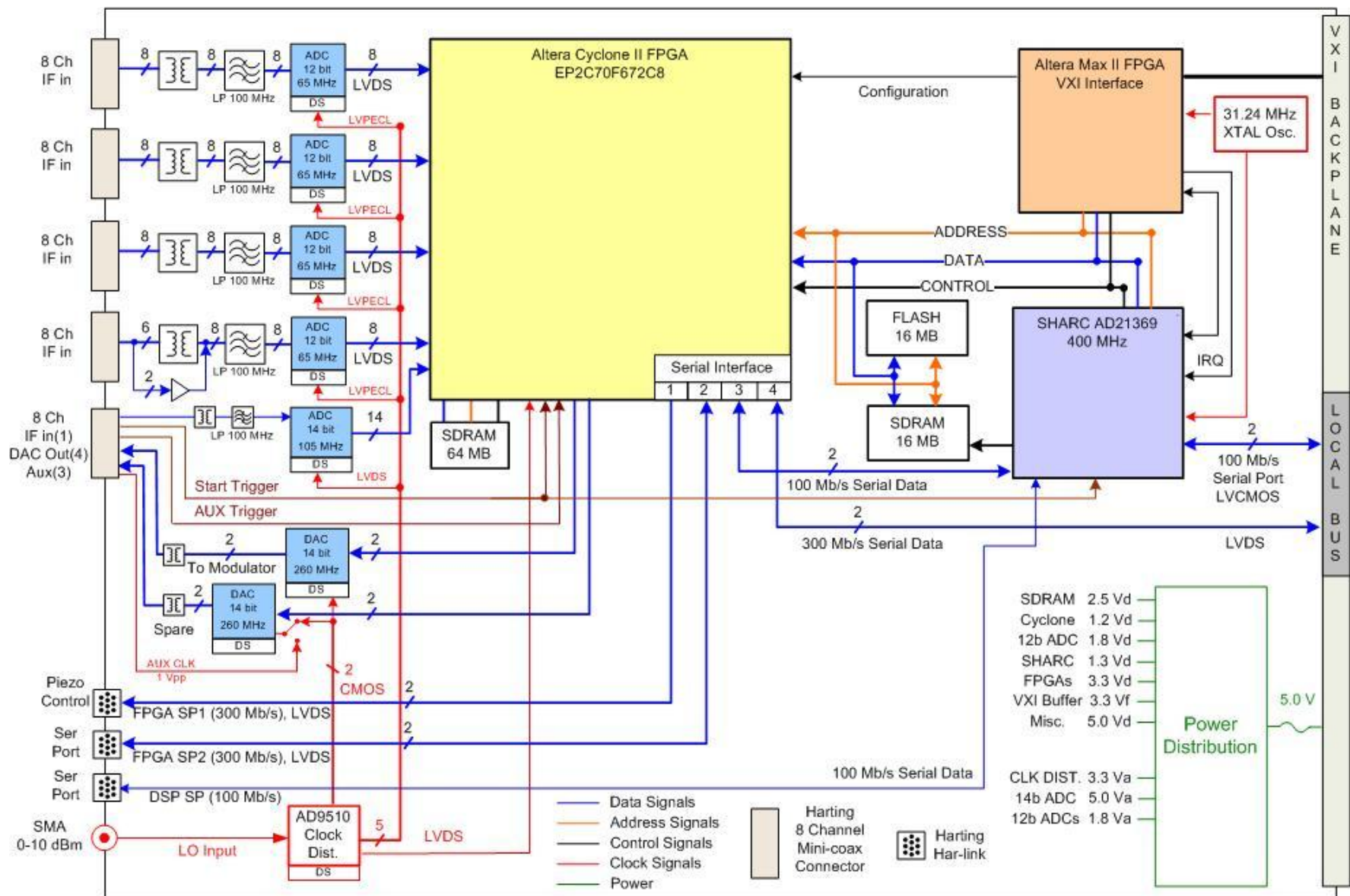
**SOFTWARE TRIGGER
OR BREAKPOINT TRIGGER**



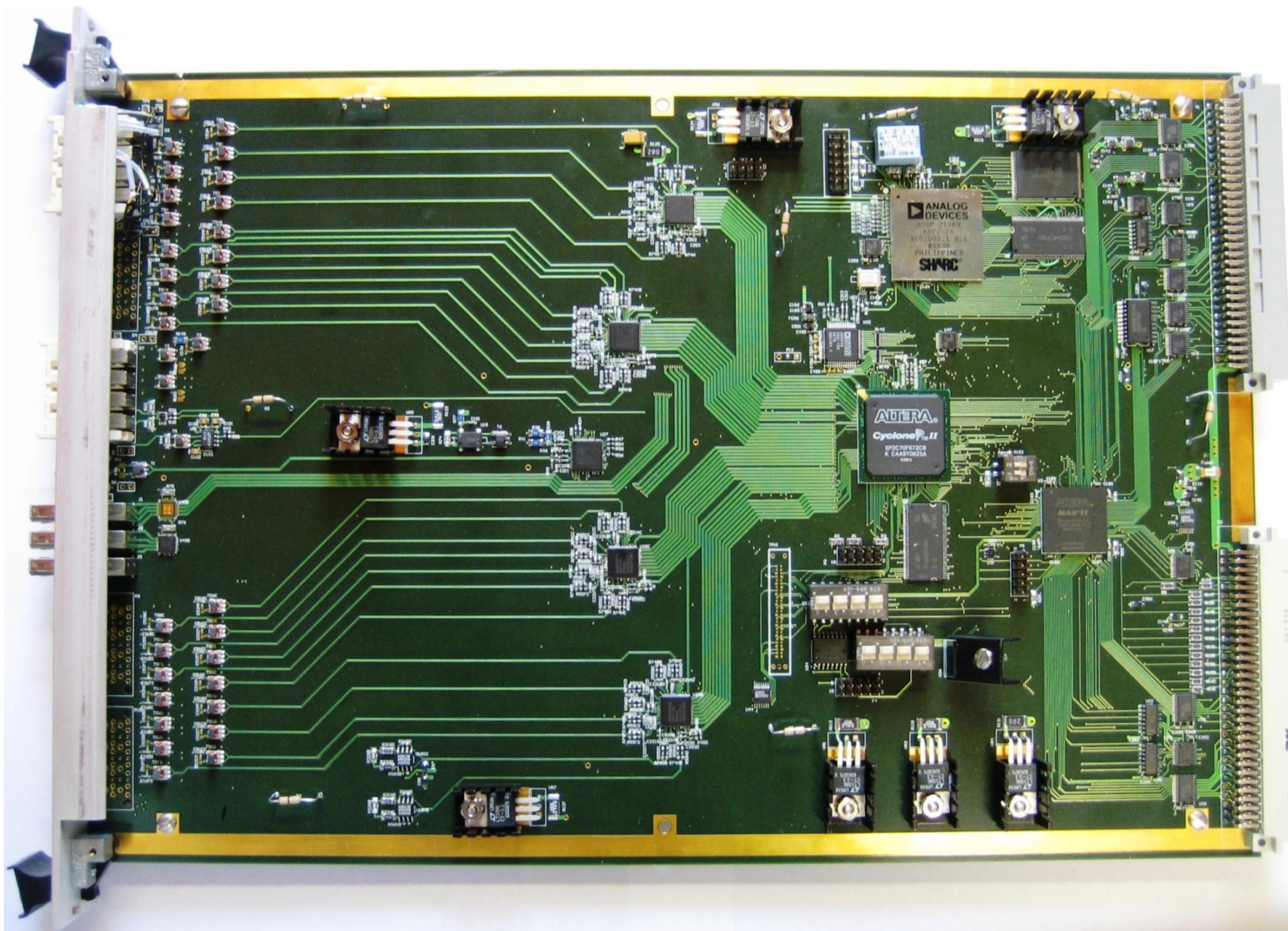
LLRF System Example



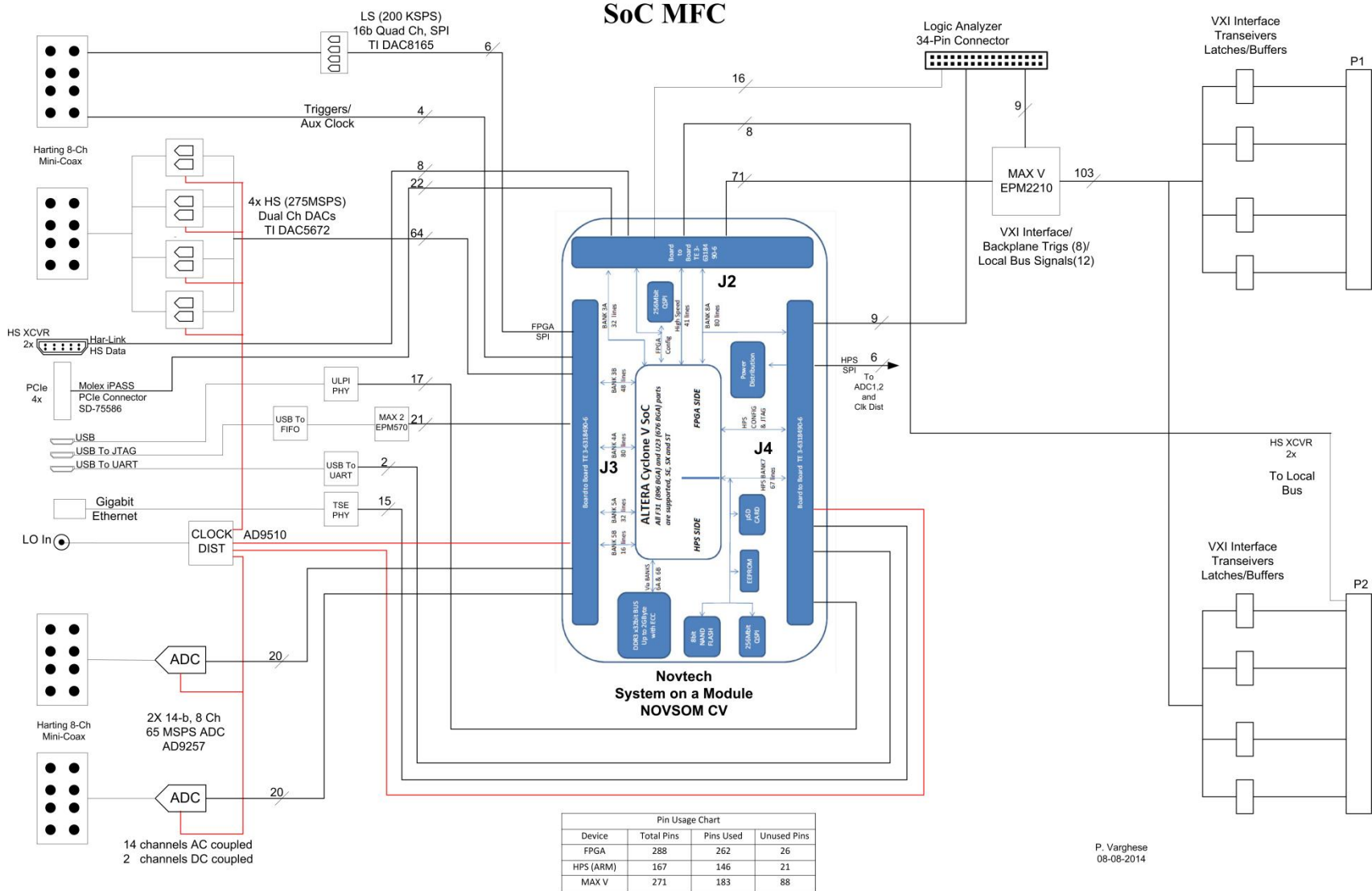
Cyclone II based MFC (2007)



33 ADC ch, 4 DAC ch

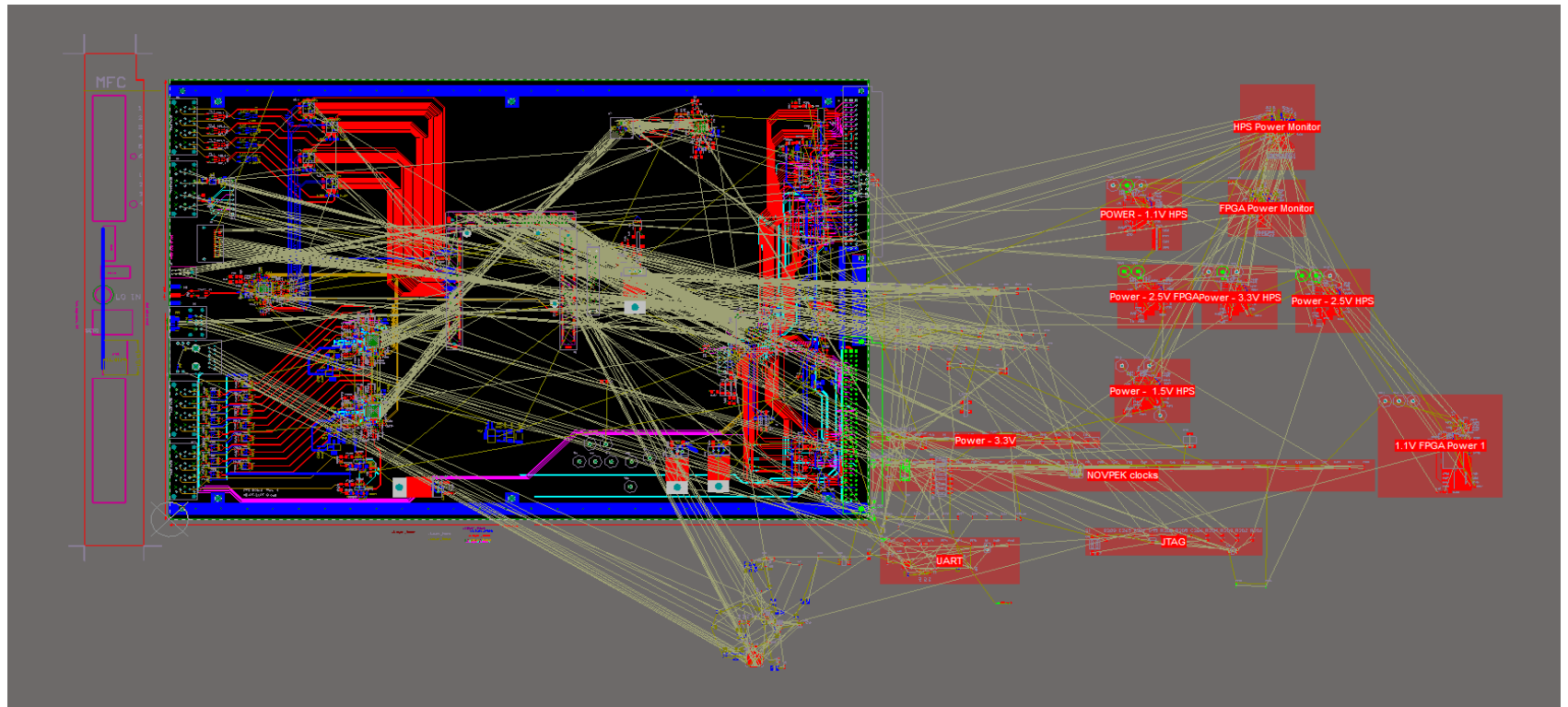


SoC Cyclone V SOM based MFC (2014)

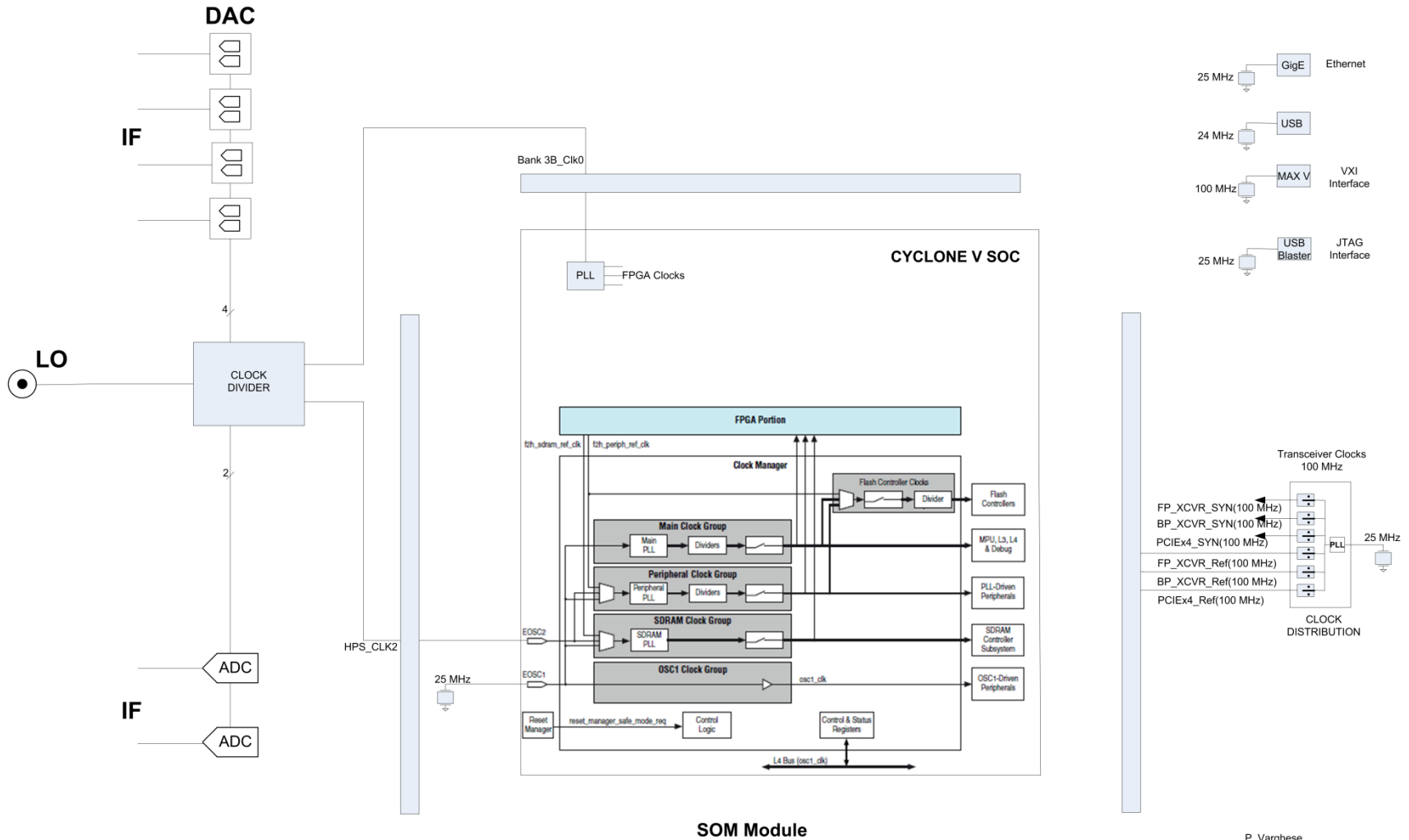


[illegible]

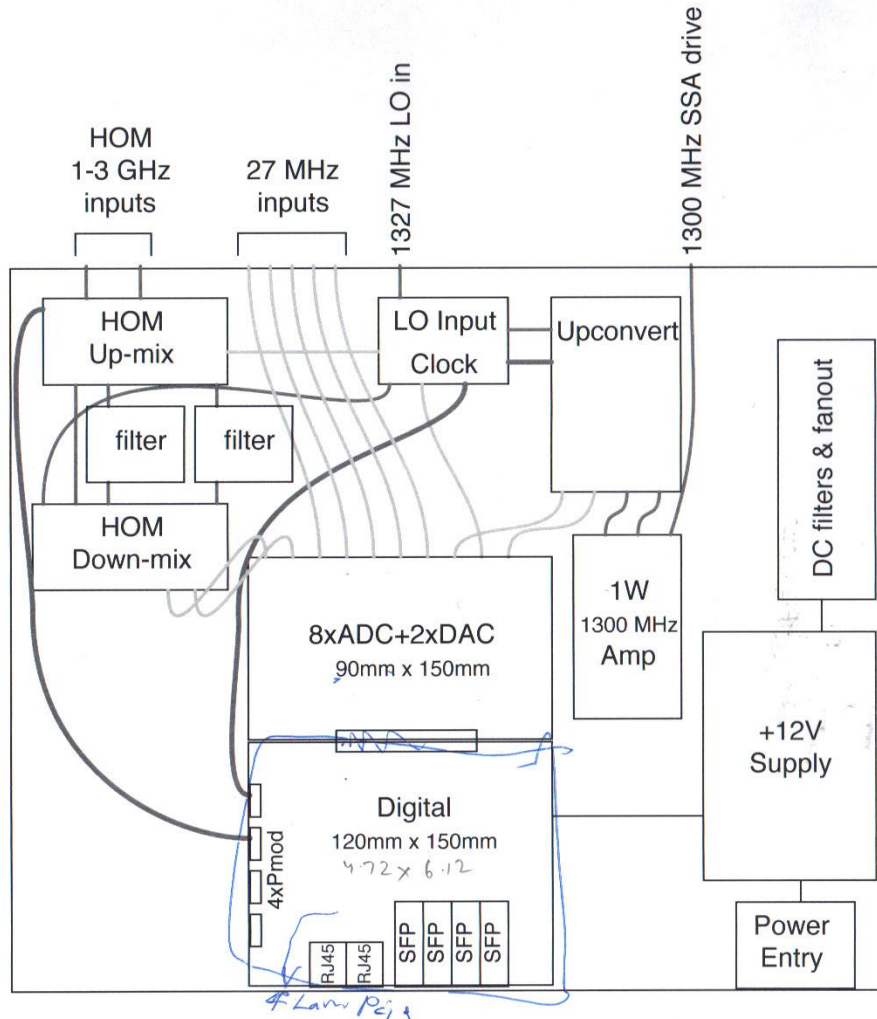
Layout ~ 2/3 Completed



SoC MFC Clock Domains



Cavity Controller



1U 19" chassis

17" x 14"

0.25" Al plate 2.6 kg

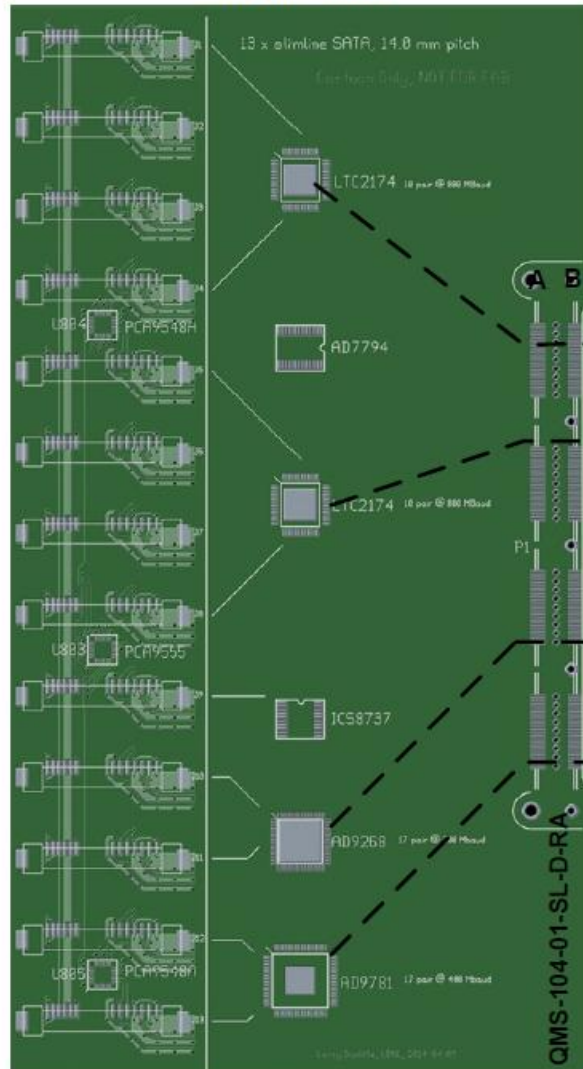
Passively cooled ~30W

— Coax >1GHz

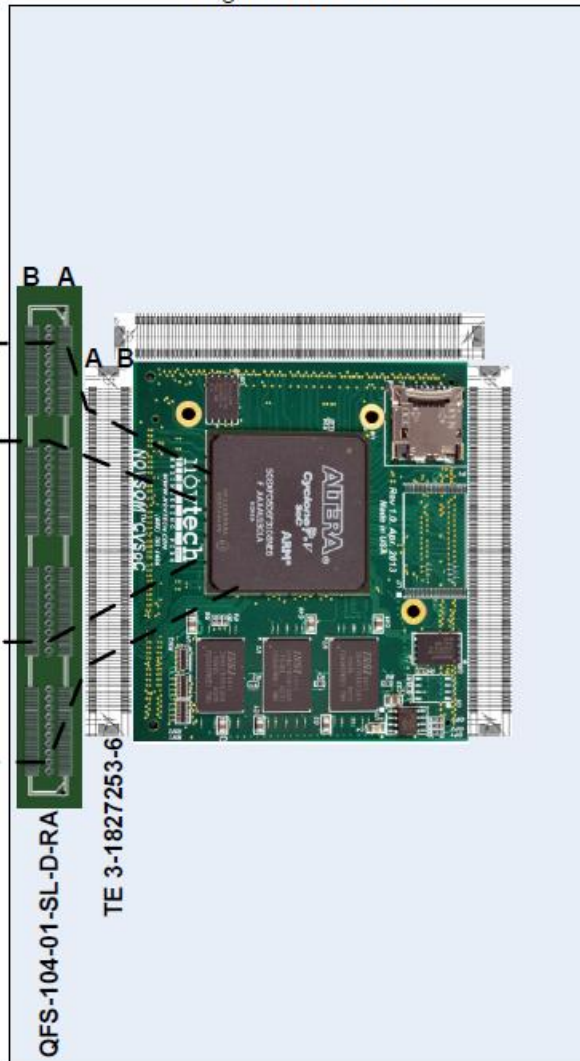
— Coax <1GHz

— Pmod ribbon

ADC/DAC Board



Digital/FPGA Board



ADC/DAC Pin Assignments

QMS-104 (ADC Brd)	QFS-104 (FPGA Brd)
A1 SCL	FPGA_SCL
A2 GND	
A3 SDA	FPGA_SDA
A4 VALUX	FPGA_3.3V
A5 GND	
A6 W01A	LTC2174_1_OUT1A_P
A7 W01B	LTC2174_1_OUT1A_N
A8 GND	
A9 W02A	LTC2174_1_OUT2A_P
A10 W02B	LTC2174_1_OUT2A_N
A11 GND	
A12 W03A	LTC2174_1_DCO_P
A13 W03B	LTC2174_1_DCO_N
A14 GND	
A15 W04A	LTC2174_1_OUT3A_P
A16 W04B	LTC2174_1_OUT3A_N
A17 GND	
A18 W05A	LTC2174_1_OUT4A_P
A19 W05B	LTC2174_1_OUT4A_N
A20 GND	
A21 W06A	LTC2174_2_OUT1A_P
A22 W06B	LTC2174_2_OUT1A_N
A23 GND	
A24 W07A	LTC2174_2_OUT2A_P
A25 W07B	LTC2174_2_OUT2A_N
A26 GND	
C1 VIO	FPGA_2.5V
C2 GND	
C3 W15A	LTC2174_2_DCO_P
C4 W15B	LTC2174_2_DCO_N
C5 GND	
C6 W16A	LTC2174_2_OUT3A_P
C7 W16B	LTC2174_2_OUT3A_N
C8 GND	
C9 W17A	LTC2174_2_OUT4A_P
C10 W17B	LTC2174_2_OUT4A_N
C11 GND	
C12 W18A	FPGA_SPI_SDO
C13 W18B	FPGA_SPI_SDI
C14 GND	
C15 W19A	FPGA_SPI_CLK
C16 W19B	
C17 GND	
C18 W20A	CLK_P

QMS-104 (ADC Brd)	QFS-104 (FPGA Brd)
B1 GND	
B2 VBULK	FPGA_5.0V
B3 VBULK	FPGA_5.0V
B4 GND	
B5 W08A	LTC2174_1_OUT1B_P
B6 W08B	LTC2174_1_OUT1B_N
B7 GND	
B8 W09A	LTC2174_1_OUT2B_P
B9 W09B	LTC2174_1_OUT2B_N
B10 GND	
B11 W10A	LTC2174_1_FR_P
B12 W10B	LTC2174_1_FR_N
B13 GND	
B14 W11A	LTC2174_1_OUT3B_P
B15 W11B	LTC2174_1_OUT3B_N
B16 GND	
B17 W12A	LTC2174_1_OUT4B_P
B18 W12B	LTC2174_1_OUT4B_N
B19 GND	
B20 W13A	LTC2174_2_OUT1B_P
B21 W13B	LTC2174_2_OUT1B_N
B22 GND	
B23 W14A	LTC2174_2_OUT2B_P
B24 W14B	LTC2174_2_OUT2B_N
B25 GND	
B26 VIO	FPGA_2.5V
D1 GND	
D2 W23A	LTC2174_2_FR_P
D3 W23B	LTC2174_2_FR_N
D4 GND	
D5 W24A	LTC2174_2_OUT3B_P
D6 W24B	LTC2174_2_OUT3B_N
D7 GND	
D8 W25A	LTC2174_2_OUT4B_P
D9 W25B	LTC2174_2_OUT4B_N
D10 GND	
D11 W26A	LTC2174_1_SPI_CS
D12 W26B	LTC2174_2_SPI_CS
D13 GND	
D14 W27A	AD9268_SPI_CS
D15 W27B	AD9781_SPI_CS
D16 GND	
D17 W28A	
D18 W28B	

C19 W20B	CLK_N
C20 GND	
C21 W21A	
C22 W21B	
C23 GND	
C24 W22A	AD9268_D0_N
C25 W22B	AD9268_D0_P
C26 GND	
E1 W00E	
E2 GND	
E3 W31A	AD9268_D3_N
E4 W31B	AD9268_D3_P
E5 GND	
E6 W32A	AD9268_D4_N
E7 W32B	AD9268_D4_P
E8 GND	
E9 W33A	AD9268_D6_N
E10 W33B	AD9268_D6_P
E11 GND	
E12 W34A	AD9268_D8_N
E13 W34B	AD9268_D8_P
E14 GND	
E15 W35A	AD9268_D9_N
E16 W35B	AD9268_D9_P
E17 GND	
E18 W36A	AD9268_D11_N
E19 W36B	AD9268_D11_P
E20 GND	
E21 W37A	AD9268_D13_N
E22 W37B	AD9268_D13_P
E23 GND	
E24 W38A	AD9268_D15_N
E25 W38B	AD9268_D15_P
E26 GND	
G1 VIO	FPGA_2.5V
G2 GND	
G3 W47A	AD9781_D12_P
G4 W47B	AD9781_D12_N
G5 GND	
G6 W48A	AD9781_D10_P
G7 W48B	AD9781_D10_N
G8 GND	
G9 W49A	AD9781_D8_P
G10 W49B	AD9781_D8_N
G11 GND	

D19 GND	
D20 W29A	
D21 W29B	
D22 GND	
D23 W30A	
D24 W30B	
D25 GND	
D26 W00D	
F1 GND	
F2 W39A	AD9268_D1_N
F3 W39B	AD9268_D1_P
F4 GND	
F5 W40A	AD9268_D3_N
F6 W40B	AD9268_D3_P
F7 GND	
F8 W41A	AD9268_D5_N
F9 W41B	AD9268_D5_P
F10 GND	
F11 W42A	AD9268_D7_N
F12 W42B	AD9268_D7_P
F13 GND	
F14 W43A	AD9268_DCO_N
F15 W43B	AD9268_DCO_P
F16 GND	
F17 W44A	AD9268_D10_N
F18 W44B	AD9268_D10_P
F19 GND	
F20 W45A	AD9268_D12_N
F21 W45B	AD9268_D12_P
F22 GND	
F23 W46A	AD9268_D14_N
F24 W46B	AD9268_D14_P
F25 GND	
F26 VIO	FPGA_2.5V
H1 GND	
H2 W55A	AD9781_D13_P
H3 W55B	AD9781_D13_N
H4 GND	
H5 W56A	AD9781_D11_P
H6 W56B	AD9781_D11_N
H7 GND	
H8 W57A	AD9781_D9_P
H9 W57B	AD9781_D9_N
H10 GND	
H11 W58A	AD9781_D7_P

G12 W50A	AD9781_D6_P
G13 W50B	AD9781_D6_N
G14 GND	
G15 W51A	AD9781_DCI_P
G16 W51B	AD9781_DCI_N
G17 GND	
G18 W52A	AD9781_D4_P
G19 W52B	AD9781_D4_N
G20 GND	
G21 W53A	AD9781_D2_P
G22 W53B	AD9781_D2_N
G23 GND	
G24 W54A	AD9781_D0_P
G25 W54B	AD9781_D0_N
G26 GND	

H12 W58B	AD9781_D7_N
H13 GND	
H14 W59A	AD9781_DCI_P
H15 W59B	AD9781_DCI_N
H16 GND	
H17 W60A	AD9781_D5_P
H18 W60B	AD9781_D5_N
H19 GND	
H20 W61A	AD9781_D3_P
H21 W61B	AD9781_D3_N
H22 GND	
H23 W62A	AD9781_D1_P
H24 W62B	AD9781_D1_N
H25 GND	
H26 SCLR	FPGA_SCLR

Digital Board Completion

